DOCKET NO.: END919980110US3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Jimarez *et al.*	)	Examiner: Berezny, Nema O.
	)	
Serial No.: 09/782,471	)	
	)	Art Unit: 2813
Filed: 2/12/01	)	
	)	

For: FLIP CHIP C4 EXTENSION STRUCTURE AND PROCESS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Request for Re-Instatement of Appeal Under 37 CFR §1.93(b)(2)

Applicants request Re-Instatement of the Appeal from the rejection of the Examiner dated October 22, 2002, in light of the Office Action mailed August 6, 2003. Submitted herewith is a Supplemental Appeal Brief which addresses the rejection of claims in the Office Action mailed August 6, 2003.

Respectfully submitted,

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Commissioner for Patents
Washington, D.C. 20231

SUPPLEMENTAL BRIEF OF APPELLANTS

This Supplemental Appeal Brief, pursuant to the Office Action mailed August 6, 2003, 2003, is an appeal from the rejection of the Examiner dated October 22, 2002. The Appeal Brief filed April 22, 2003 is incorporated, in its entirety, herein by reference. The present Supplemental Appeal Brief addresses the rejections of claims in the Office Action mailed August 6, 2003.

REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-18 and 40-41 are currently pending. Claims 19-39 are withdrawn from consideration. Claims 1-18 and 40-41 have been rejected. This Brief is in support of an appeal from the rejection of claims 1-18 and 40-41.

STATUS OF AMENDMENTS

There are no After-Final Amendments which have not been entered.

SUMMARY OF INVENTION

As illustrated in FIGS. 7-8, the present invention discloses an electrical structure, comprising: a first substrate; first and third conductive bodies mechanically and electrically coupled to the first substrate; and a nonsolderable and nonconductive material volumetrically surrounding and contacting a first portion of a surface of the first conductive body such that a second portion of the surface of the first conductive body is not contacted by the nonsolderable and nonconductive material. The nonsolderable and nonconductive material volumetrically surrounds and contacts a first portion of a surface of the third conductive body such that a second portion of the surface of the third conductive body is not contacted by the nonsolderable and nonconductive material,. The nonsolderable and nonconductive material is continuously distributed between the first conductive body and the third conductive body. See FIGS. 7-8; see also FIGS. 1-4 and description thereof in the specification on page 10, line 16 - page 13, line 1. The electrical structure further comprises second and fourth conductive bodies mechanically and electrically coupled to a second substrate. See FIGS. 7-8; see also FIGS. 5-6 and description

thereof in the specification on page 13, line 2 - page 14, line 16. The second conductive body mechanically and electrically coupled to the first conductive body by surface adhesion at between a surface of the second conductive body and the second portion of the surface of the first conductive body , and the a fourth conductive body mechanically and electrically coupled to the third conductive body by surface adhesion between a surface of the fourth conductive body and the second portion of the surface of the third conductive body. See FIG 8; specification, page 16, lines 10-13. A melting point of the second conductive body is less than a melting point of the first conductive body; and a melting point of the fourth conductive body is less than a melting point of the third conductive body. See specification, page 13, lines 10-12.

The first conductive body may include a solder bump. See specification, page 13, line 3. The height of the second conductive body may be at least about 50% of a height of the solder bump. See specification, page 20, line 20 - page 21, line 2.

An area of the first portion of the surface of the first conductive body may exceed an area of the second portion of the surface of the first conductive body by a factor of at least about 10. See specification, page 18, lines 2-5.

A second conductive body may be at least about 3 mils. See specification, page 21, line 2.

The nonsolderable and nonconductive material may be selected from the group consisting of a polyimide, a photosensitive resin, an epoxy, and a silicone. See specification, page 11, lines 16-17; page 35, lines 9-12.

The electrical structure may further comprise an encapsulating material between the nonsolderable and nonconductive material and the second substrate, wherein the encapsulating

material encapsulates the second conductive body. See specification, page 18, lines 12-16. The encapsulating material may include epoxy anhydride with silica filler. See specification, page 42, lines 12-15.

The melting point of first conductive body may exceed the melting point of the second conductive body by no more than about 147 °C. See specification, page 11, lines 8-11.

The second conductive body may include lead and tin in a eutectic lead/tin ratio. See specification, page 13, lines 12-15. However, the second conductive body may include lead and tin in lead/tin ratio that exceeds a eutectic lead/tin ratio. See specification, page 13, lines 15-17.

The substrate may includes an organic or ceramic material. See specification, page 16, lines 4-9.

The electrical structure may further comprise a second nonsolderable and nonconductive coating material, wherein a first portion of a surface of the second conductive body is coated by the second nonsolderable and nonconductive coating material such that a second portion of the surface of the second conductive body is not contacted by the second nonsolderable and nonconductive coating material, and wherein the second portion of the surface of the second conductive body is mechanically and electrically coupled to the second portion of the surface of the first conductive body. The second nonsolderable and nonconductive coating material includes a cured light-sensitive resin. See FIG. 6; specification, page 14, lines 4-16.

The first substrate may includes a chip or a module. See specification, page 11, line 11. and the second substrate may include a chip carrier or a circuit card. See specification, page 13, lines 7-8.

The nonsolderable and nonconductive material may be rigid at a temperature that is equal

to the melting point of the first conductive body, and the nonsolderable and nonconductive material is rigid at a temperature that is equal to the melting point of the third conductive body. See specification, page 15, line 18 - page 16, line 4.

ISSUES

1. Whether claims 1-6, 9-11, 13-14, 16-18, and 40-41 under 35 U.S.C. §103(a) are unpatentable over Somaki et al. (U.S. Patent 5,641,113) in view of Akamatsu et al. (U.S. Patent 5,611,481).

2. Whether claims 7-8, 12, and 15 under 35 U.S.C. §103(a) are unpatentable over Somaki (U.S. Patent 5,641,113) in view of Akamatsu (U.S. Patent 5,611,481), and further in view of Thomas (U.S. Patent 6,213,347).

GROUPING OF CLAIMS

The claims are grouped as shown in Table 1:

Table 1

Group	Issue	Claims	Do Claims of Group Rise or Fall Together?
1	1	1-3, 5-6, 14, 16-18, 40-41	Yes
2	1	4, 9-11, 13	No
3	2	7-8	Yes
4	2	12, 15	No

Groups 1-2 includes the claims corresponding to Issue 1. Groups 3-4 includes the claims corresponding to Issue 2. The claims of Groups 1-2 (associated with Issue 1) do not rise and fall

together with the claims of Groups 3-4 (associated with Issue 2), because the claims of Groups 1-2 and the claims of Groups 3-4 are rejected over different combinations of references.

Claims of Groups 1-2

Table 1 shows that: the claims of Group 1 stand and fall together. The claims of Group 2 do not stand and fall together, as shown in Table 1, because each of claims 4, 9-11, and 13 in Group 2 raises a unique issue not raised by any of the other claims in Group 2.

Claim 4 raises the unique issue of whether the cited references teach or suggest the following feature of claim 4: "wherein an area of the first portion of the surface of the first conductive body exceeds an area of the second portion of the surface of the first conductive body by a factor of at least about 10".

Claim 9 raises the unique issue of whether the cited references teach or suggest the following feature of claim 9: "wherein the melting point of first conductive body exceeds the melting point of the second conductive body by no more than about 147 °C".

Claim 10 raises the unique issue of whether the cited references teach or suggest the following feature of claim 10: "wherein the second conductive body includes lead and tin in a eutectic lead/tin ratio".

Claim 11 raises the unique issue of whether the cited references teach or suggest the following feature of claim 11: "wherein the second conductive body includes lead and tin in lead/tin ratio that exceeds a eutectic lead/tin ratio".

Claim 13 raises the unique issue of whether the cited references teach or suggest the following feature of claim 13: "wherein the second substrate includes a ceramic material".

The claims of Group 2 do not rise and fall together with the claims of any of Group 1, because the claims 4, 9-10, and 13 in Group 2 raise issues or features (recited *supra*) which do not arise in connection with any of the claims of Group 1.

Claims of Groups 3-4

Table 1 shows that: the claims of Group 3 stand and fall together. The claims of Group 4 do not stand and fall together, as shown in Table 1, because each of claims 12 and 15 in Group 4 raises a unique issue not raised by any of the other claims in Group 3.

Claim 12 raises the unique issue of whether the cited references teach or suggest the following feature of claim 12: "wherein the second substrate includes an organic material".

Claim 15 raises the unique issue of whether the cited references teach or suggest the following feature of claim 15: "wherein the second nonsolderable and nonconductive coating material includes a cured light-sensitive resin".

The claims of Group 4 do not rise and fall together with the claims of any of Group 3, because the claims 12 and 15 in Group 4 raise issues or features (recited *supra*) which do not arise in connection with any of the claims of Group 3.

ARGUMENT

Issue 1

CLAIMS 1-6, 9-11, 13-14, 16-18, AND 40-41 UNDER 35 U.S.C. §103(A) ARE NOT UNPATENTABLE OVER SOMAKI ET AL. (U.S. Patent 5,641,113) IN VIEW OF AKAMATSU ET AL. (U.S. Patent 5,611,481).

The Examiner rejected claims 1-6, 9-11, 13-14, 16-18, and 40-41 under 35 U.S.C. §103(a) as being unpatentable over Somaki (5,641,113) in view of Akamatsu (5,611,481).

Claims 1 and 18

Applicants respectfully contend that claims 1 and 18 are not unpatentable over Somaki in view of Akamatsu based on any of several arguments.

A first argument that claims 1 and 18 are not unpatentable over Somaki in view of Akamatsu relates to the coupling between the first and third conductive bodies 13a FIGS. 2A-2E and 3 of Somaki (as identified by the Examiner) and the second and fourth conductive bodies 13b in FIGS. 2E and 3 of Somaki (as identified by the Examiner), respectively, in Somaki. Claim 1 requires: "a second conductive body mechanically and electrically coupled to the first conductive body by **surface adhesion** at between a surface of the second conductive body and the second portion of the surface of the first conductive body" and "a fourth conductive body mechanically and electrically coupled to the third conductive body by **surface adhesion** between a surface of the fourth conductive body and the second portion of the surface of the third conductive body" (emphasis added). Claim 18 similarly recites: "means for mechanically and

electrically coupling the second conductive body to the first conductive body by **surface adhesion** between a surface of the second conductive body and the second portion of the surface of the first conductive body" and "means for mechanically and electrically coupling the fourth conductive body to the third conductive body by **surface adhesion** between a surface of the fourth conductive body and the second portion of the surface of the third conductive body" (emphasis added).

Appellants contend that Somaki does not teach or suggest said surface adhesion between the solder bumps 13a and the respective solder bumps 13b. Moreover, said surface adhesion is physically impossible in the Somaki, by virtue of the disclosure in col. 6, lines 47-50 of Somaki which states: "In FIG. 2E, the **boundary lines** between the solder bumps 13a and 13b are actually **invisible** by reason that the solder bumps 13a and 13b are **molten and mixed** each other in this embodiment" (emphasis added). Appellants contend that said mixing of the molten solder effectively destroys the respective surfaces of the solder bumps 13a and 13b, so that it is physically impossible for the solder bumps 13a and 13b to be mechanically coupled to each other by surface adhesion. Said mixing of the molten solder creates a volumetric interface between the solder bumps 13a and 13b, said volumetric interface comprising solder from both the solder bump 13a and the solder bump 13b, said volumetric interface serving to mechanically couple the solder bumps 13a and 13b with each other.

A second argument that claims 1 and 18 are not unpatentable over Somaki in view of Akamatsu relates to the Examiner's rationale for combining Somaki and Akamatsu based on the Examiner's allegation that Akamatsu discloses that the melting point of the second conductive body is less than the melting point of the first conductive body as required by claims 1 and 18.

The Examiner admits that "Somaki does not disclose a second conductive body whose melting point is less than a melting point of said first conductive body." The Examiner argues that "Akamatsu discloses a flip chip device wherein the chip is coupled to the substrate using two stacked layers of conductive bodies wherein the melting point of one conductive body exceeds the melting point of a second conductive body by no more than about 147 degrees C (col.4 lines 4-16). Akamatsu also discloses a eutectic lead/tin ratio conductive body and a lead/tin ratio conductive body that exceeds a eutectic lead/tin ratio (col.4 lines 4-16), and a ceramic substrate (col.5 lines 25-31). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the conductive bodies of different melting points of Akamatsu such as eutectic and non-eutectic conductive bodies, and the ceramic substrate of Akamatsu with the electrical structure of Somaki in order to avoid repellency of molten soldering metal by the electrode surface and thereby reduce electric resistance and increase mechanical strength of the connection (Akamatsu col.3 line 48 - colA line 27), and to utilize a thermally conductive substrate, respectively."

In response to the preceding argument by the Examiner for combining Somaki and Akamatsu, Appellants point to the specific teachings of Akamatsu.

> "Referring to FIG. 1B, a connection part made of an eutectic alloy consisting of the first metal component and the second metal component is formed between the first soldering metal bump and the second soldering metal bump by heating the both soldering metal bumps at a temperature lower than the melting temperature of the first metal component to maintain the first soldering metal bump in a solid phase at an interface with the aluminum electrode and then cooling down to solidify both of the bumps before the eutectic reaction reaches the aluminum electrode pad 2, in order **to prevent the aluminum electrode pad from repelling the first soldering metal bump.**"
>
> Referring to FIG. 2A, a semiconductor chip 1 has **an electrode pad 2 of aluminum has repellency against molten metal.** The first soldering metal bump 3A is formed on the

> electrode pad 2 in a trapezoidal shape by deposition technique using a mask having an opening with the same pattern as the first electrode pad, while a circuit board 6 has an electrode pad 5 of copper has adhesive tendency to molten metal. The second soldering metal bump 4A is formed on the electrode pad 5. A melting temperature of the first soldering metal bump is higher than that of the second soldering metal bump."

(emphasis added) Akamatsu, col. 3, lines 48-59. Akamatsu further recites:

> "The electric connection implemented in the first and second embodiments described above does not have disconnection failure **due to repellency of molten soldering metal by the electrode surface** in the fabrication process. That reduces electric resistance and increases mechanical strength of the connection."

(emphasis added). Akamatsu, col. 4, lines 22-27.

Applicants maintain that the preceding quotes from Akamatsu do not teach or suggest that use of conductive bodies of different melting points (i.e., the melting point of the second conductive body is less than the melting point of the first conductive body) avoids repellency of molten soldering metal by the electrode surface. To the contrary, Akamatsu discloses that the issue of repellency of molten soldering metal by the electrode surface is controlled by the electrode material (and thus by the melting point of the second conductive body being less than the melting point of the first conductive body, as alleged by the Examiner). In particular, Akamatsu discloses, that such repellency of molten soldering metal by the electrode surface occurs if the electrode is made of aluminum (see Akamatsu, col. 3, lines 32-35) and does not occur if the electrode is made of copper (see Akamatsu, col. 3, lines 35-38). This is a non-issue in Somaki, since Somaki does not disclose use of an electrode made of a material (e.g., aluminum) that repels molten solder. The only electrode material exposed to molten solder disclosed by Somaki is copper (see Somaki, col. 1, line 64 - col. 2, line 1), and Somaki describes said copper as "wettable" which is consistent with Akamatsu's assertion that copper adhesively

attracts molten copper. Therefore, Appellants respectfully contend that it is not obvious to modify Somaki with the teaching of Akamatsu for the purpose of avoiding repelling molten solder, since there is no repellency of molten solder in Somaki in the absence of incorporating the teaching of Akamatsu. Thus, the Examiner's argument for combining Somaki and Akamatsu is not persuasive.

Additionally, Somaki already enjoys the benefit alleged by the Examiner, said benefit allegedly resulting from combining Akamatsu with Somaki, and thus Somaki does not need what Akamatsu allegedly offers. In particular, Somaki recites on col. 4, line 64 - col. 5, line 2: "In operation, temperatures in the oven and conveyor speed are controlled adequately to solder the solder baits onto the external electrodes 12 at 230 degrees C. After the reflowing step, solder bumps 13a are formed and **engaged abuttingly** corresponding external electrodes 12, as shown in FIG. 2B" (emphasis added). Thus Somaki already has a good mechanical and electrical connection between the solder bumps 13a and the external electrodes 12, without any help from Akamatsu. Therefore, the Examiner's rationale for combining Somaki and Akamatsu is not persuasive.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 18 are not unpatentable over Somaki in view of Akamatsu, and that claims 1 and 18 are in condition for allowance.

Claim 2

Since claim 2 depends from claim 1, which Appellants have argued *supra* to be

patentable under 35 U.S.C. §103(a), Appellants maintain that claim 2 is not unpatentable under 35 U.S.C. §103(a).

Claim 3

Since claim 3 depends from claims 1 and 2, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 3 is not unpatentable under 35 U.S.C. §103(a).

Claim 4

Since claim 4 depends from claims 1 and 2, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 4 is not unpatentable under 35 U.S.C. §103(a).

Additionally, Somaki in view of Akamatsu does not teach or suggest the feature: "wherein an area of the first portion of the surface of the first conductive body exceeds an area of the second portion of the surface of the first conductive body by a factor of at least about 10" as required by claim 4.

The Examiner argues: "Somaki specifically discloses an area of said first portion exceeding an area of said second portion by a factor of over 5 (col.5 lines 3-4, 48-51). Somaki also discloses that said areas of covered and exposed regions is a tradeoff between the area of the electrodes and the volume of the solder balls (col.9 lines 38-50). Therefore, it would have been obvious and within reasonable experimentation for a person skilled in the art at the time of the invention to adjust the volume and the exposed circular area of the solder balls to meet specific

product demands. For example, Somaki discloses an exposed area diameter of 0.63 mm and a sphere diameter of 0.8 mm (col.5 lines 3-4, 48-51), which results in a ratio of covered area to exposed area of approximately 5.5. If the exposed diameter was changed to 0.6 mm and the sphere volume was changed to 1.0 mm, said ratio would be 10.1. If the exposed diameter was changed to 0.5 and the sphere volume was changed to 0.9, said ratio would be 12.0."

In response to the preceding argument by the Examiner, Appellants note that the Examiner has made an invalid argument; i.e., the Examiner has argued that "said areas of covered and exposed regions is a tradeoff between the area of the electrodes and the volume of the solder balls (col.9 lines 38-50)," which is incorrect. In fact, Somaki teaches:

> "In the present invention, how large the top portion 15 or 35 is formed is a trade-off between a solder bump height and a diameter of the constricted part of the solder joints. Preferably, the area of the exposed top portion 15 or 35, as in the embodiments, is formed as the same area as that of the external electrode 12, for its formation avoids being concentrated the shear strain into one of the constricted parts of each solder joint. The area of the external electrodes 12 and the volume of the solder balls are determined in consideration of the trade-off."

Somaki, col. 9, lines 38-47. The preceding quote from Somaki shows that the area of the external electrodes 12 and the volume of the solder balls are determined as a consequence of the trade-off, and do not constitute the tradeoff itself as alleged by the Examiner. Indeed, Somaki disclosed that there is a "trade-off between a solder bump height and a diameter of the constricted part of the solder joints". The Examiner has not presented an analysis based on the preceding tradeoff. Therefore, the Examiner's analysis, being based on an incorrect assumption of what the tradeoff is, and not taking into account what the correct tradeoff actually is, is not persuasive.

In consideration of the Examiner having performed an analysis based on an incorrect

assumption, together with the Examiner's admission that Somaki specifically discloses a ratio of covered area to exposed area of approximately 5.5 which does not satisfy the ratio of at least 10 required by claim 4, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 4. Therefore, Appellants maintain that claim 4 is not unpatentable over Somaki in view of Akamatsu.

Claim 5

Since claim 5 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 5 is not unpatentable under 35 U.S.C. §103(a).

Claim 6

Since claim 6 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 6 is not unpatentable under 35 U.S.C. §103(a).

Claim 9

Since claim 9 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 9 is not unpatentable under 35 U.S.C. §103(a).

Additionally, Somaki in view of Akamatsu does not teach or suggest "wherein the melting point of first conductive body exceeds the melting point of the second conductive body

by no more than about 147 °C" as required by claim 9.

The Examiner's alleges that "Akamatsu discloses a flip chip device wherein the chip is coupled to the substrate using two stacked layers of conductive bodies wherein the melting point of one conductive body exceeds the melting point of a second conductive body by no more than about 147 degrees C (col.4 lines 4-16). Akamatsu also discloses a eutectic lead/tin ratio conductive body and a lead/tin ratio conductive body that exceeds a eutectic lead/tin ratio (col.4 lines 4-16), and a ceramic substrate (col.5 lines 25-31). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the conductive bodies of different melting points of Akamatsu such as eutectic and non-eutectic conductive bodies, and the ceramic substrate of Akamatsu with the electrical structure of Somaki in order to avoid repellency of molten soldering metal by the electrode surface and thereby reduce electric resistance and increase mechanical strength of the connection (Akamatsu col.3 line 48 - colA line 27), and to utilize a thermally conductive substrate, respectively."

In response to the preceding argument by the Examiner, Appellants contend that the preceding reason given by the Examiner for combining Akamatsu with Somaki is irrelevant to the melting point temperature differential of no more than about 147 °C as claimed by claim 9. Thus, the Examiner's argument for combining Akamatsu with Somaki does not establish a *prima facie* case of obviousness with respect to the preceding feature of claim 9.

In addition, the Examiner's argument depends on the Examiner's assumption that combining Akamatsu with Somaki solves an electrode repellency problem in Somaki's invention. However, Appellants have argued *supra* in relation to claim 1 that Somaki does not have the electrode repellency problem alleged by the Examiner. Thus, Appellants contend that

the Examiner's argument for modifying Somaki with the teaching of Akamatsu in relation to claim 9 is not persuasive. Therefore, claim 9 is not unpatentable under 35 U.S.C. §103(a).

Claims 10-11

Since claims 10-11 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claims 10-11 are not unpatentable under 35 U.S.C. §103(a).

Additionally, Somaki in view of Akamatsu does not teach or suggest the feature: "wherein the second conductive body includes lead and tin in a eutectic lead/tin ratio" as required by claim 10. Also, Somaki in view of Akamatsu does not teach or suggest the feature: "wherein the second conductive body includes lead and tin in lead/tin ratio that exceeds a eutectic lead/tin ratio" as required by claim 11.

The Examiner alleges: "Akamatsu also discloses a eutectic lead/tin ratio conductive body and a lead/tin ratio conductive body that exceeds a eutectic lead/tin ratio (col.4 lines 4-16), and a ceramic substrate (col.5 lines 25-31). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the conductive bodies of different melting points of Akamatsu such as eutectic and non-eutectic conductive bodies, and the ceramic substrate of Akamatsu with the electrical structure of Somaki in order to avoid repellency of molten soldering metal by the electrode surface and thereby reduce electric resistance and increase mechanical strength of the connection (Akamatsu col.3 line 48 - colA line 27), and to utilize a thermally conductive substrate, respectively.".

In response to the preceding argument by the Examiner, Appellants contend that the

preceding reason given by the Examiner for combining Akamatsu with Somaki is irrelevant to whether the lead/tin ratio is a eutectic lead/tin ratio or in excess of a eutectic lead/tin ratio. Thus, the Examiner's argument for combining Akamatsu with Somaki does not establish a *prima facie* case of obviousness with respect to the preceding feature of claims 10-11.

In addition, the Examiner's argument depends on the Examiner's assumption that combining Akamatsu with Somaki solves an electrode repellency problem in Somaki's invention. However, Appellants have argued *supra* in relation to claim 1 that Somaki does not have the electrode repellency problem alleged by the Examiner. Thus, Appellants contend that the Examiner's argument for modifying Somaki with the teaching of Akamatsu in relation to claims 10-11 is not persuasive. Therefore, claims 10-11are not unpatentable under 35 U.S.C. §103(a).

<u>Claim 13</u>

Since claim 13 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 13 is not unpatentable under 35 U.S.C. §103(a).

Additionally, Somaki in view of Akamatsu does not teach or suggest the feature: "wherein the second substrate includes a ceramic material" as required by claim 13. The Examiner alleges that Akamatsu teaches the preceding feature of claim 13.

The Examiner's alleges that "Akamatsu discloses a flip chip device wherein the chip is coupled to the substrate using two stacked layers of conductive bodies wherein the melting point of one conductive body exceeds the melting point of a second conductive body by no more than

about 147 degrees C (col.4 lines 4-16). Akamatsu also discloses a eutectic lead/tin ratio conductive body and a lead/tin ratio conductive body that exceeds a eutectic lead/tin ratio (col.4 lines 4-16), and a ceramic substrate (col.5 lines 25-31). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the conductive bodies of different melting points of Akamatsu such as eutectic and non-eutectic conductive bodies, and the ceramic substrate of Akamatsu with the electrical structure of Somaki in order to avoid repellency of molten soldering metal by the electrode surface and thereby reduce electric resistance and increase mechanical strength of the connection (Akamatsu col.3 line 48 - colA line 27), and to utilize a thermally conductive substrate, respectively."

In response to the preceding argument by the Examiner, Appellants contend that the preceding reason given by the Examiner for combining Akamatsu with Somaki is irrelevant to whether the substrate includes a ceramic material. Thus, the Examiner's argument for combining Akamatsu with Somaki does not establish a *prima facie* case of obviousness with respect to the preceding feature of claims 10-11.

In addition, the Examiner's argument depends on the Examiner's assumption that combining Akamatsu with Somaki solves an electrode repellency problem in Somaki's invention. However, Appellants have argued *supra* in relation to claim 1 that Somaki does not have the electrode repellency problem alleged by the Examiner. Thus, Appellants contend that the Examiner's argument for modifying Somaki with the teaching of Akamatsu in relation to claim 13 is not persuasive. Therefore, claim 13 is not unpatentable under 35 U.S.C. §103(a).

Claim 14

Since claim 14 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 14 is not unpatentable under 35 U.S.C. §103(a).

Claim 16

Since claim 16 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 16 is not unpatentable under 35 U.S.C. §103(a).

Claim 17

Since claim 17 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 17 is not unpatentable under 35 U.S.C. §103(a).

Claim 40

Since claim 40 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 40 is not unpatentable under 35 U.S.C. §103(a).

Claim 41

Since claim 41 depends from claim 18, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 41 is not unpatentable under

35 U.S.C. §103(a).

Issue 2

CLAIMS 7-8, 12, AND 15 UNDER 35 U.S.C. §103(A) ARE NOT UNPATENTABLE OVER SOMAKI IN (U.S. Patent 5,641,113) VIEW OF AKAMATSU (U.S. Patent 5,611,481), AND FURTHER IN VIEW OF THOMAS (6,213,347).

The Examiner rejected claims 7-8, 12, and 15 under 35 U.S.C. §103(a) as being unpatentable over Somaki in view of Akamatsu, and further in view of Thomas (6,213,347).

Claim 7

Since claim 7 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 7 is not unpatentable under 35 U.S.C. §103(a).

Claim 8

Since claim 8 depends from claims 1 and 7, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 8 is not unpatentable under 35 U.S.C. §103(a).

Claim 12

Since claim 12 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 12 is not unpatentable under

35 U.S.C. §103(a).

Additionally, Somaki in view of Akamatsu and further in view of Thomas does not teach or suggest the feature: "wherein the second substrate includes an organic material" as required by claim 12.

The Examiner argues: "Somaki in view of Akamatsu do not disclose an encapsulating material which includes epoxy anhydride with silica filler, an organic substrate, or a cured light-sensitive resin material. Thomas discloses a flip chip device which comprises an encapsulating material between the chip and attached substrate, which includes epoxy anhydride with silica filler and cured by light irradiation (col.5 lines 62-67; col.6 lines 23-28; col.7 lines 1-3; col.8 line 65 col.8 line 3). Thomas also discloses an organic substrate (col.5 lines 62-67). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the encapsulant and organic substrate of Thomas with the electronic structure of Somaki and Akamatsu in order to distribute and absorb stress caused by the different CTE's of the different materials in the structure (Thomas col.7 lines 28-35)."

In response to the preceding argument by the Examiner, Appellants contend that the preceding reason given by the Examiner for combining Akamatsu with Somaki is irrelevant to whether the second substrate includes an organic material as required by claim 12. The encapsulant referred to by the Examiner is not comprised by the second substrate as required by claim 12, but instead fills the gap between the first substrate (i.e., the chip) and the second substrate. See description of FIG. 1 in Thomas, col. 5, lines 9-12 ("FIG 1 is a simplified and schematic cross section of an integrated circuit chip attached to a substrate using solder balls, with the gap between chip and substrate filled with a polymeric encapsulant"). See also,

Thomas, col. 6, lines 23-28 ("The gap 16 is filled with a polymeric encapsulant 18 that extends over the printed circuit board about the perimeter of the chip. The main purpose of encapsulant 18, commonly referred to as the "underfill" material, is a reduction of mechanical stress in the assembly; another purpose is the protection of the active chip surface.").

Since the encapsulant is not comprised by the second substrate, as required by claim 12, Appellants contend that the Examiner's argument is not persuasive. Additionally, Thomas does not teach or suggest that the encapsulant must comprise an organic material in order to reduce mechanical stress.

Accordingly, Appellants maintain that the Examiner has not established a *prima facie* case of obviousness with respect to the preceding feature of claim 12. Therefore, claim 12 is not unpatentable under 35 U.S.C. §103(a).

Claim 15

Since claim 15 depends from claims 1 and 14, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 15 is not unpatentable under 35 U.S.C. §103(a). Additionally, Somaki in view of Akamatsu and further in view of Thomas does not teach or suggest the feature: "wherein the second nonsolderable and nonconductive coating material includes a cured light-sensitive resin" as required by claim 15.

The Examiner alleges that Thomas discloses that the encapsulating material includes epoxy anhydride with silica filler and cured by light irradiation. The Examiner argues: "A light cured resin avoids the need to heat the entire package in order to cure the resin".

In response to the preceding argument by the Examiner, Appellants contend that it is not

obvious to use a light-sensitive resin in order to avoid heating the entire package in order to cure the resin. As stated in Somaki, col. 5, lines 5-42, the package is heated to a low temperature of only 150 °C, which is below the melting temperature of the solder. Thus the heating of the entire package is non-destructive. With a light-sensitive resin, the resin would be cured through absorption of light at an appropriate wavelength, which may be a more expensive process than use of elevated temperature. Additionally, a light-sensitive resin may be more expensive than is a material that is thermally curable. The Examiner has not provided an analysis to show that curing by light is an advantage to curing by heat.

Accordingly, Appellants maintain that the Examiner has not established a *prima facie* case of obviousness with respect to the preceding feature of claim 15. Therefore, claim 15 is not unpatentable under 35 U.S.C. §103(a).

SUMMARY

In summary, Appellants respectfully request reversal of the rejection under 35 U.S.C. §103(a) of claims 1-18 and 40-41.

Respectfully submitted,

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Applicants: Jimarez *et al.*	)	Examiner: Berezny, Nema O.
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For: FLIP CHIP C4 EXTENSION STRUCTURE AND PROCESS

Commissioner for Patents
Washington, D.C. 20231

APPENDIX - CLAIMS ON APPEAL

1. An electrical structure, comprising:

a first substrate;

a first conductive body mechanically and electrically coupled to the first substrate;

a third conductive body mechanically and electrically coupled to the first substrate;

a nonsolderable and nonconductive material, wherein the nonsolderable and nonconductive material volumetrically surrounds and contacts a first portion of a surface of the first conductive body such that a second portion of the surface of the first conductive body is not contacted by the nonsolderable and nonconductive material, wherein the nonsolderable and nonconductive material volumetrically surrounds and contacts a first portion of a surface of the third conductive body such that a second portion of the surface of the third conductive body is not contacted by the nonsolderable and nonconductive material, and wherein the nonsolderable

and nonconductive material is continuously distributed between the first conductive body and the third conductive body;

a second conductive body mechanically and electrically coupled to the first conductive body by surface adhesion at between a surface of the second conductive body and the second portion of the surface of the first conductive body, wherein a melting point of the second conductive body is less than a melting point of the first conductive body;

a fourth conductive body mechanically and electrically coupled to the third conductive body by surface adhesion between a surface of the fourth conductive body and the second portion of the surface of the third conductive body, wherein a melting point of the fourth conductive body is less than a melting point of the third conductive body; and

a second substrate mechanically and electrically coupled to both the second conductive body and the fourth conductive body.

2. The electrical structure of claim 1, wherein the first conductive body includes a solder bump.

3. The electrical structure of claim 2, wherein a height of the second conductive body is at least about 50% of a height of the solder bump.

4. The electrical structure of claim 2, wherein an area of the first portion of the surface of the first conductive body exceeds an area of the second portion of the surface of the first conductive body by a factor of at least about 10.

5. The electrical structure of claim 1, wherein a height of the second conductive body is at least about 3 mils.

6. The electrical structure of claim 1, wherein the nonsolderable and nonconductive material selected from the group consisting of a polyimide, a photosentive resin, an epoxy, and a silicone.

7. The electrical structure of claim 1, further comprising an encapsulating material between the nonsolderable and nonconductive material and the second substrate, wherein the encapsulating material encapsulates the second conductive body.

8. The electrical structure of claim 7, wherein the encapsulating material includes epoxy anhydride with silica filler.

9. The electrical structure of claim 1, wherein the melting point of first conductive body exceeds the melting point of the second conductive body by no more than about 147 °C.

10. The electrical structure of claim 1, wherein the second conductive body includes lead and tin in a eutectic lead/tin ratio.

11. The electrical structure of claim 1, wherein the second conductive body includes lead and tin in lead/tin ratio that exceeds a eutectic lead/tin ratio.

12. The electrical structure of claim 1, wherein the second substrate includes an organic material.

13. The electrical structure of claim 1, wherein the second substrate includes a ceramic material.

14. The electrical structure of claim 1, further comprising a second nonsolderable and nonconductive coating material, wherein a first portion of a surface of the second conductive body is coated by the second nonsolderable and nonconductive coating material such that a second portion of the surface of the second conductive body is not contacted by the second nonsolderable and nonconductive coating material, and wherein the second portion of the surface of the second conductive body is mechanically and electrically coupled to the second portion of the surface of the first conductive body.

15. The electrical structure of claim 14, wherein the second nonsolderable and nonconductive coating material includes a cured light-sensitive resin.

16. The electrical structure of claim 1, wherein the first substrate includes a chip, and wherein the second substrate includes a chip carrier or a circuit card.

17. The electrical structure of claim 1, wherein the first substrate includes a chip or a module, and wherein the second substrate includes a circuit card.

18. An electrical structure, comprising:

a first substrate;

a first conductive body mechanically and electrically coupled to the first substrate;

a third conductive body mechanically and electrically coupled to the first substrate;

a nonsolderable and nonconductive material, wherein the nonsolderable and nonconductive material volumetrically surrounds and contacts a first portion of a surface of the first conductive body such that a second portion of the surface of the first conductive body is not contacted by the nonsolderable and nonconductive material, wherein the nonsolderable and nonconductive material volumetrically surrounds and contacts a first portion of a surface of the third conductive body such that a second portion of the surface of the third conductive body is not contacted by the nonsolderable and nonconductive material, and wherein the nonsolderable and nonconductive material is continuously distributed between the first conductive body and the third conductive body;

a second conductive body, wherein a melting point of the second conductive body is less than a melting point of the first conductive body;

means for mechanically and electrically coupling the second conductive body to the first conductive body by surface adhesion between a surface of the second conductive body and the second portion of the surface of the first conductive body;

a fourth conductive body, wherein a melting point of the fourth conductive body is less than a melting point of the third conductive body;

means for mechanically and electrically coupling the fourth conductive body to the third conductive body by surface adhesion between a surface of the fourth conductive body and the

second portion of the surface of the third conductive body; and

a second substrate mechanically and electrically coupled to both the second conductive body and the fourth conductive body.

40. The electrical structure of claim 1, wherein the nonsolderable and nonconductive material is rigid at a temperature that is equal to the melting point of the first conductive body, and wherein the nonsolderable and nonconductive material is rigid at a temperature that is equal to the melting point of the third conductive body.

41. The electrical structure of claim 18, wherein the nonsolderable and nonconductive material is rigid at a temperature that is equal to the melting point of the first conductive body, and wherein the nonsolderable and nonconductive material is rigid at a temperature that is equal to the melting point of the third conductive body.